Chair of Integrated Digital Systems and Circuit Design

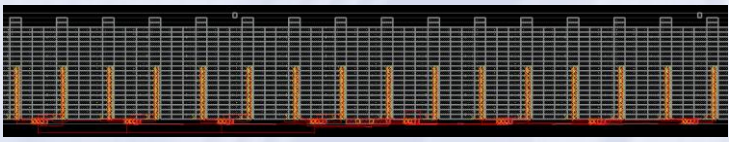
RWTH AACHEN UNIVERSITY

Research Activity (HiWi, Master/Bachelor Thesis)

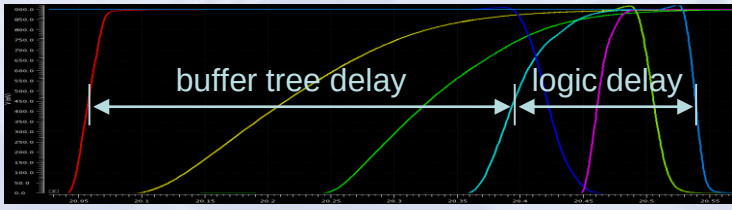
Automated Design Space Exploration and Buffer Tree Optimization

The maximum clock frequency of digital signal processing circuits is determined by the critical path delay between successive pipeline registers. In complex circuits the critical path can be constituted by logic gates in the data path as well as buffer trees for large fan-out signals. An example digital circuit is shown in the figures on the right (top: layout view of the input buffer tree topology, bottom: break down of the critical path delay). Therefore, both the logic depth as well as the structure of the buffer trees require careful optimization for challenging speed requirements. The technique of *Structured Datapath* (SDP) description enables the structured optimization of cell selection and placement in a standard cell design flow.

This work aims at the modeling and optimization of buffer trees in order to support the design space exploration of digital circuits. An abstract yet reliable delay & energy model is required for the quick assessment of alternative buffer tree configurations. Based on this model optimization strategies (e.g. simulated annealing) are to be applied. Finally, SDP-compatible descriptions of selected optimal buffer trees should be generated automatically for given specifications.



Floorplan of VLSI macro with highlighted input buffer tree



Critical path delay composed of buffer tree and logic path delay

Tasks

1. Develop a script to determine delay and energy consumption for a given buffer tree;
2. Elaborate optimization strategies for buffer tree minimizing delay and/or energy;
3. Implement the automated generation of optimized buffer tree descriptions suitable for SDP design;
4. Implement an abstract model for the design space exploration considering buffer trees and logic paths.

Requirements

1. Programming experience, e. g. MATLAB, C, perl, or python;
2. Basic understanding of digital circuit design;
3. Experience in HDL programming is a plus;
4. Self-motivated;
5. Knowledge of English (spoken and written).

Contact

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