Chair of Integrated Digital Systems and Circuit Design

RWTH AACHEN UNIVERSITY

Master Thesis

Low-Voltage SRAM Design Optimization under Process Variations

Voltage scaling techniques are widely applied to reduce power consumption in modern SoCs. The minimum energy point (MEP) is typically reached at near/sub-threshold operation. Hence, low-voltage operation is considered a key design concept especially to enable the upcoming era of ubiquitous Internet-of-Things (IoT) and further promote wearable technologies. As opposed to conventional circuit design operating at nominal supply voltages with a considerable margin to the threshold voltage, subthreshold designs run a voltages below it. This dramatically shrinks noise margins and as a result faces great challenges due process variations and random fluctuations.

Taking SRAM circuits as an example, the suited candidate will study optimizations for near- and sub-threshold operation considering nanometer technologies. More specifically, the objective is to address reliability issues of low-voltage SRAMs, from a perspective of circuits design in a systematic and in-depth fashion. The minimum access voltages for read/write operations and the data retention voltage will be taken as design targets. The trade-off between area, energy and reliability will be quantized. Putting in place a combined effort on analytical modeling, circuit simulation and design optimization, the study is expected to advance the state-of-the art in energy-efficient and reliable design of low-voltage SRAMs.

This work offers a great opportunity for students to gain in-depth knowledge and hands-on experiences in two specific areas: subthreshold design as well as SRAM design. This will also entail scripting and running circuit simulations.

Tasks

1. Literature reviews on low-voltage design and SRAM design: theoretical background, circuits design solutions, key features for subthreshold SRAM operation;

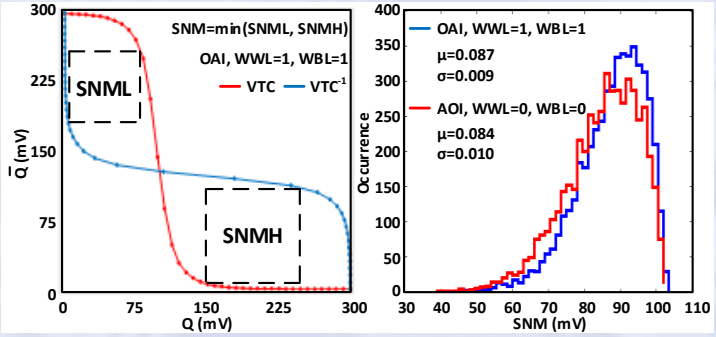

Fig. 1. Simulations of SRAM static noise margin (SNM).

2. Characterizations of subthreshold operation features, including subthreshold swing factors and DIBL-effect coefficients, etc., on advanced CMOS process nodes by SPICE simulations;

3. Static noise margin (SNM) simulations on SRAM bit-cells in subthreshold region, and characterizations of SNM distributions in different operation modes under process variations;

4. Developments of SNM model for subthreshold SRAM based on I-V relationships of MOS transistors and the model validation in simulations;

5. Studies on subthreshold SRAM optimization based on the developed SNM models to explore the SRAM design tradeoff between e.g., area, energy and reliability beyond the state-of-the-art.

Requirements

1. Strong knowledge on circuits design and good skills on transistor-level circuit simulations;
2. Sound mathematical background for circuit modeling and analysis;
3. Basic knowledge on SRAM design or low-voltage design or Perl/TCL scripting will be a plus;
4. Self-motivated
5. Good English in writing and speaking

Contact

Prof. Dr.-Ing. Tobias Gemmeke
gemmeke@ids.rwth-aachen.de
+49 241 80 97600

Dr.-Ing. Xin Fan
fan@ids.rwth-aachen.de
+49 241 80 97606